Amendment to the Specification

Paragraph starting in page 4, line 2

B2

Figure 1 illustrated a transmitter 100 used according to the V.92 standard in accordance with the present invention. The transmitter 100 includes a modulus encoder 105, a precoder 110, a prefilter 115, a convolutional encoder 120, and an inverse map 125. The modulus encoder 105 is a standard multiple modulus encoder. The modulus encoder 105 receives and encodes a block of bits $b_0:b_{k-1}$. The block of bits $b_0:b_{k-1}$ is represented as an integer R_0. The output signal is a set of numbers $K_0:K_{l-1}$ derived from R_0 as the multiple modulus representation of R_0. This output is then mapped into equivalence classes u(n) in order to minimize the power coming out of the precoder. The equivalence classes u(n) are related to each other in a simple manner as in classical Tomlinson precoding. Thus, the expanded constellations have points labeled in blocks from 0 to M_{i-1}, where M_i is the modulus for the ith constellation.

Paragraph starting in page 6, line 18

B3

The process 200 of correcting for a phase shift is shown in Figure ~~2~~ 2A. The process begins at a start state-205. Proceeding to state ~~210~~ 210a, the process ~~200~~ 200a determines the sign of the frame value. One technique to determine the sign of the frame is using the following formula:

Paragraph starting in page 7, line 1

B4

After determining the sign, the process 200 proceeds to state ~~210~~ 215a. In state ~~210~~ 215a, the process 200 differentially encodes the sign of the frame. The sign may be differentially encoded using the formula:

Paragraph starting in page 7, line 6

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B5

The process 200 then proceeds to state ~~220~~ 220a. In state ~~220~~ 220a, the process 200 differentially encodes the frame. The frame may be differentially encoded using techniques known to one of skill in the art. For example, the frame may be differentially encoded using the formula:

Paragraph starting in page 7, line 16

B6

Proceeding to state ~~230~~ 230a, the process 200 determines the sign of the output. The sign of the output is 0 if the channel output is equal to or less than half the product of the moduli and 1 if the channel output is more than half the product of the moduli. This relationship can be stated as follows:

Paragraph starting in page 8, line 1

B7

Proceeding to state ~~235~~ 235a, the process 200 differentially decodes the output. The output may be differentially decoded using the following formula:

$$R_0 = [N + (-1)^{r(n-1)} R(n)]_{\mathrm{mod}\, N}.$$

After the output is differentially decoded, the process 200 is invariant to 180 degree phase shifts. Thus, the process 200 concludes in end state 240.

Paragraph starting in page 8, line 8

B8

Referring now to Figure 2B. ~~An~~ an example of the process 200 will now be provided. The example is for a 3 symbol multiple modulus encoder with moduli of 7, 3 and 10. The product of these moduli is 210, so 7 bits can be mapped in each frame. Let the inputs, in decimal, be 86, 45, 112, and 103.

Paragraph starting in page 8, line 13

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B9

First, the sign stream is determined according to state ~~210~~ 210b. One-half the product of the moduli is (210/2), or 105. Thus, the inputs less than or equal to 105 are given a sign of 0 and those greater than 105 are given a sign of 1. This creates an original sign stream is 0, 0, 1, 0.

Paragraph starting in page 8, line 18

B10

After determining the original sign stream, the sign stream is differentially encoded according to state 215b. The differentially encoded sign stream is 0, 0, 1, 1. Applying this to the inputs we get new inputs to the modulus converter of 86, 45, 112, 107 (-103 + 210) as shown in state 217b. As shown in state 220b, ~~This~~ this new input is then differentially encoded, resulting in a differentially encoded stream is of 86, 131, 33 (131 + 112 – 210), 140. This stream translates into symbols of {2, 2, 6}, {4, 1, 1}, {1, 0, 3}, {4, 2, 0}

Paragraph starting in page 9, line 3

B11

If the channel does not have phase inversion, the symbols 86, 131, 33, 140 arrive which are differentially decoded into 86, 45, 112, 107, as shown in state 225b. The sign pattern 0, 0, 1, 1 is differentially decoded into 0, 0, 1, 0, as shown in state 230b. As shown in states 235b, 237b, ~~The~~ the differentially decoded sign pattern is then applied to the outputs of the multiple modulus decoder differential decoder, resulting in the correct final stream of 86, 45, 112, 103 (-107 + 210).

Paragraph starting in page 9, line 10

B12

If the channel is subject to phase inversion, the symbols arrive as {4 (7-1-2), 0, (3-1-2), 3 (10-1-6}, {2,1,8}, {5, 2, 6}, {2, 0, 9} as also shown in state 225b. These symbols decode to 123, 78, 176, 69. These symbols are differentially decoded to produce 124 (123 – 209 (an inverter 0) + 210), 165 (78 – 123 + 210), 98, 103 as shown in state 235b. The sign pattern of the decoded symbols is 1, 1, 0, 0, which differentially decodes to 0, 0, 1, 0. Applying this to the multiple

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B12 cont

modulus decoder differential decoder gives the values 86 (-124 + 210), 45, 112, 103, as shown in state 237b.

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